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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,079	12/01/2003	Hisao Takahashi	7465-US-1	4790

7590 01/10/2005

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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,079	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4 and 9-12* is/are allowed.

6)☒ Claim(s) *5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2000* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/01/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-12 are presented in the instant application according to the Applicants' filing on 12/01/2003.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Inventorship

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (U. S. Patent No. 5,880,612).

With respect to claim 5, Kim discloses, in Fig. 2, a circuit and its corresponding jitter inducing method comprising the steps of a) setting delay times [232] for rising and/or falling edges of pulses in a reference pulse train [234] for sequential interval of the reference pulse train, and b) providing pulses of the reference pulse train [234] in order of the corresponding intervals wherein delays are applied to the rising and/or falling edges of the pulses by said delay time [232] being set every interval.

With respect to claim 6, Kim discloses, in Fig. 2, that the changes of the delay time over the intervals are a function of a delayed time transition waveform [216/218].

With respect to claim 7, Kim discloses, in Fig. 2, a circuit and its corresponding pulse generating method for providing a pulse train derived from a reference pulse train [234] divided into sequential intervals wherein delay times [232] applied to rising and/or falling edges of pulses in the reference pulse train are set interval by interval, and the changes of the delay times over the sequential intervals are controlled to be a desired function.

With respect to claim 8, Kim discloses, in Fig. 2, that the delay times [232] are controlled according to the desired function determined by parameters designated through a user interface [MAX DELAY SELECT].

Allowable Subject Matter

5. Claims 1-4 and 9-12 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A jitter inducing circuit including a switch control means for controlling a switch means to provide pulses to one delay means in which a setup of a delay time has finished, as called for in claim 1;

b) A jitter inducing method including steps of switching the supply of a reference pulse train to a second delay block from a first delay block and delaying the reference pulse train by the second delay block and providing an output to an output terminal, as called for in claim 9;

c) A circuit for generating a pulse train, in which a pulse providing means for providing a pulse to be jittered and a pulse not to be jittered to separate delay blocks of the plurality of delay blocks wherein both pulses are derived from a reference pulse train, and the delay times for the delay block to which the non-jittered pulse is provided is fixed, and the delay time of the delay block to which the pulse to be jittered is provided changes sequentially, as called for in claim 11; and

d) A pulse generating method including the steps of (a) delaying rising edge or falling edge of a pulse to be jittered according to a preset delay time and (b) composing a non-jittered pulse and the pulse delayed in step (a), as called for in claim 12.

Citation of Relevant Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Iwasa et al. (U.S. Patent No. 5,327,411) discloses a write control method in a circuit having a first delay and a second delay and a control signal generating circuit.

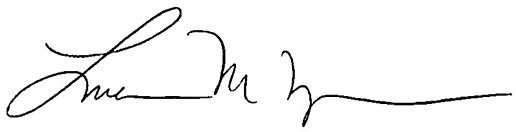
Prior art Kaplinsky (U.S. Patent No. 5,298,866) discloses a clock distribution circuit with active de-skewing.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



LMN

LINH MY NGUYEN
PRIMARY EXAMINER